

Refine Search

Search Results -

Terms	Documents
L2 and (((user adj1 programmable) or programmable) adj1 connector)	27

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L3

[Refine Search](#)[Recall Text](#)[Clear](#)[Interrupt](#)

Search History

DATE: Monday, December 05, 2005 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*L3 L2 and (((user adj1 programmable) or programmable) adj1 connector)L2 L1 near10 ("static random access memory" or SRAM)L1 "field programmable gate array" or FPGA

Hit Count Set Name

result set

27 L31086 L222921 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 and (((user adj1 programmable) or programmable) adj1 connector)	0

Database:

US Pre-Grant Publication Full-Text Database

US Patents Full-Text Database

US OCR Full-Text Database

EPO Abstracts Database

JPO Abstracts Database

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Search:

L4

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Monday, December 05, 2005 [Printable Copy](#) [Create Case](#)

<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side			result set
<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L4</u>	L2 and (((user adj1 programmable) or programmable) adj1 connector)	0	<u>L4</u>
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L3</u>	L2 and (((user adj1 programmable) or programmable) adj1 connector)	27	<u>L3</u>
<u>L2</u>	L1 near10 ("static random access memory" or SRAM)	1086	<u>L2</u>
<u>L1</u>	"field programmable gate array" or FPGA	22921	<u>L1</u>

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(716/16 710/100 710/305 710/316 710/300 710/313 711/104 365/185.01 365/185.11 326/37 326/38 326/39).ccls.	8795

Database:

US Pre-Grant Publication Full-Text Database
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Search:

L5

Refine Search

Recall Text

Clear

Interrupt

Search History

 DATE: Monday, December 05, 2005 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5 710/100,305,316,300,313;326/37-39;365/185.01,185.11;711/104;716/16.ccls.

8795

L5

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L2 and (((user adj1 programmable) or programmable) adj1 connector)

0

L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L2 and (((user adj1 programmable) or programmable) adj1 connector)

27

L3

L2 L1 near10 ("static random access memory" or SRAM)

1086

L2

L1 "field programmable gate array" or FPGA

22921

L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3 and L5	17

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L6

Search History

DATE: Monday, December 05, 2005 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L6 L3 and L5 17 L6

L5 710/100,305,316,300,313;326/37-39;365/185.01,185.11;711/104;716/16.ccls. 8795 L5

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L2 and (((user adj1 programmable) or programmable) adj1 connector) 0 L4

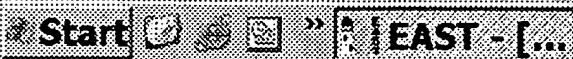
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L2 and (((user adj1 programmable) or programmable) adj1 connector) 27 L3

L2 L1 near10 ("static random access memory" or SRAM) 1086 L2

L1 "field programmable gate array" or FPGA 22921 L1

END OF SEARCH HISTORY



EAST - [Untitled1:1]

File View Edit Tools Window Help

Drafts
 BRS:
 Pending
 Active
 L1: (9637) "field progr
 L2: (667) 11 near10 ("s
 L3: (24) 12 and (((user
 L4: (22) 12 and (((use
 Failed
 Saved
 Favorites
 Tagged (0)
 UDC
 Queue
 Trash

Source List Browse Queue Clear
 DBs USPAT
 Default operator OR
☒ Plurals
☒ Highlight all hit terms initially

12 and (((user adj1 programmable) or
 programmable) adj1 connector) same (plural\$3 or
 multiple))

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Dat	Pages	Title	Current OR	Current X
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6897679 B2	20050524	46	Programmable logic array integrated circui	326/41	326/38
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6799240 B1	20040928	13	SRAM bus architecture and interconnect to an	710/305	710/100; 716/16
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6759870 B2	20040706	32	Programmable logic array integrated circui	326/41	326/38
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6417690 B1	20020709	28	Floor plan for scalable multiple level tab orie	326/41	712/37; 712/38
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6404225 B1	20020611	21	Integrated circuit incorporating a program	326/39	326/37; 326/41
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6362646 B1	20020326	14	Method and apparatus for reducing memory res	326/40	326/41; 326/47
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6326807 B1	20011204	17	Programmable logic architecture incorporat	326/40	326/38; 326/39;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6300793 B1	20011009	25	Scalable multiple level tab oriented interconne	326/41	326/47
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6292017 B1	20010918	15	Programmable logic device incorporating fu	326/40	326/38; 365/230.0
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6249143 B1	20010619	20	Programmable logic array integrated circui	326/40	326/39
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6195788	20010227	21	Mapping heterogeneous	716/18	716/16